

### **REMARKS**

In response to the Office Action of January 27, 2005, Applicants respectfully request reconsideration. Claims 1-8 were previously pending in this application. By this amendment, Applicant is canceling claim 2 without prejudice or disclaimer. Claim 1 has been amended. No new claims have been added. As a result, claims 1 and 3-8 are pending for examination with claim 1 being independent. No new matter has been added.

#### **Rejections Under 35 U.S.C. §102 and 35 U.S.C. §103**

The Office Action rejected claims 1-3 and 5-8 under 35 U.S.C. §102 as purportedly being anticipated by Abadeer et al., U.S. Patent No. 5,418,738 (Abadeer). The Office Action has also rejected claim 4 under 35 U.S.C. §103 as purportedly being unpatentable over Abadeer. Applicants respectfully traverse this rejection.

Abadeer illustrates a programmable storage element that includes a plurality of first resistors and a switching circuit for coupling the first resistors in series in response to a plurality of first controls signals. The switching circuit also couples the first resistors in parallel in response to a plurality of second control signals to permit programming of the first resistors (abstract). Abadeer describes a programmable storage element which can be programmed during a shot time period (Col. 3, lines 43-45). Abadeer further describes the programming of all the resistors being performed at once, when the resistors are coupled in parallel, as being an advantage because the required current density is achieved with a significantly lower applied voltage (Col. 7, lines 65-68).

By contrast, amended claim 1 is directed towards a multiple-level memory cell, comprising a storage element formed of several polysilicon resistors connected in series between two input/output terminals, a load in series with the resistive element, the junction point thereof forming a read terminal of the memory cell, and the respective junctions between said resistors of the storage element being accessible, and wherein certain points among said junctions of the storage element and the junction of this element with the load, are connectable, individually by a switch, either to one of said input/output terminals to the storage element, or to a terminal of application of a predetermined voltage, wherein individual programming may be performed.

Abadeer does not teach or suggest junctions of the storage element and the junction of this element with the load, are connectable, individually by a switch, either to one of said input/output terminals of the storage element, or to a terminal of application of a predetermined voltage, wherein individual programming can be performed, as recited in claim 1. As described above, Abadeer instead teaches switching a number of programmable resistors originally in series, to a parallel configuration so that programming may be performed on all the resistors at once (col. 7, lines 18-34). In fact, Abadeer teaches away from individual programming. Abadeer explains that programming the resistors coupled in parallel allows for the required programming current density to be achieved with a significantly lower applied voltage (col. 7, lines 65-68).

Claim 3-8 depend from claim 1 and are allowable for at least the same reasons. Accordingly, withdrawal of the rejections under 35 U.S.C. §102 and 35 U.S.C. §103 are respectfully requested.

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**CONCLUSION**

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,  
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